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EXAMINER	
DO, CHAT C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,587	ZABARSKI ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,13,16-24,32,33 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,13,16-24,32,33 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/21/2009.

2. Claims 1-5, 13, 16-24, 32-33 and 35-38 are pending in this application. Claims 1, 13, 17, 20, 32 and 36 are independent claims. In Amendment, claims 6-12, 14-15, 25-31 and 34 are cancelled previously. This Office Action is made non-final after a RCE filed 05/21/2009.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 13, 20-24 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (U.S. 5,726,923) in view of MacInnis et al. (U.S. 2003/0185305 A1).

Re claim 1, Okumura et al. disclose in Figures 1-9 a communications processor (e.g. architecture is seen in Figure 1) for implementing scheduling processes and reducing effort for determining a minimum value of a plurality of values stored in source registers (e.g. data field 11a in Figure 2 is stored the minimum value from either source registers 6 or 11 in Figure 1) and determining an index value of a source register having the minimum value (e.g. index field 11b in Figure 2), the communication processor

comprising: a destination register (e.g. specific register 11 in Figure 1); a first source register storing a first value (e.g. register 11 in Figure 1), wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register (e.g. Figure 2 wherein the index filed is on the upper higher bit); a second source register storing a second value (e.g. registers 5-6 in Figure 1), wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register (e.g. Figure 2 wherein the index filed is on the upper higher bit); means for comparing the first value stored in the first source register with the second value stored in the second source register (e.g. arithmetic logic unit 4 in Figure 1 as comparison unit as cited in col. 4 lines 28-40); means for storing the first value in the destination register when the first value is less than the second value (e.g. path of specific register 11 less than register 5 in Figure 3); and means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register (e.g. step S9 in Figure 3 which is done by index linking circuit 10 in Figure 1) when the second value is less than the first value (e.g. path goes through S9 in Figure 3), wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value (e.g. Figure 2 wherein the index filed is on the upper higher bits).

Okumura et al. fail to explicitly disclose (1) the condition of equal to for the first test in combine with less than to form less than or equal to; (2) the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is less than a

value of a register having an inactive status. However, MacInnis et al. disclose (2) the first source register and the second source register each include an active status bit to indicate a status of the respective register (e.g. paragraphs [0038 and 0042] as wherein the register has the status bit built-in), and wherein a value of a register having an active status is less than a value of a register having an inactive status (e.g. 0/1 as status bit whereas zero is less than one). Further, the examiner takes an Official notice that (1) the condition less than or equal is very well-known in the art and widely used in many practical applications.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add (1) the additional condition as less than or equal and (2) the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is less than a value of a register having an inactive status as seen in MacInnis et al.'s invention into Okumura et al.'s invention because it would enable to efficiently check the status and prevent unconditional event (e.g. equal result of comparison).

Re claim 2, Okumura et al. further disclose in Figures 1-9 the means for comparing, the means for storing and the means for concatenating are adapted to execute sequentially within one processor cycle (e.g. col. 4 lines 45-50 and col. 5 lines 65-68).

Re claim 3, Okumura et al. further disclose in Figures 1-9 the first source register and the destination register comprise a same register (e.g. specific register 11 in Figure 1).

Re claim 4, Okumura et al. further disclose in Figures 1-9 the second source register and the destination register comprise a same register (e.g. reversed the register 11 in Figure 1).

Re claim 5, Okumura et al. further disclose in Figures 1-9 the first value is stored in N low-order bits of the first source register and the second value is stored in N low-order bits of the second register, N being an integer value (e.g. wherein N is the size of registers 5-6 and 11 for storing the data values in Figure 1).

Re claim 13, Okumura et al. disclose in Figures 1-9 a method implemented as instructions for manipulating a network processor for implementing scheduling processes and reducing a number of network processor cycles (e.g. col. 2 lines 30-56) for determining a minimum value and a corresponding index value of a plurality of source registers of the network processor (e.g. abstract and general architecture is seen in Figure 1), the method comprising the steps of: initializing a destination register with an index value and a value of a first source register from among the plurality of source registers (e.g. Figure 2 as general data structure of each specific registers 11x in Figure 4 as repeated loop. Within the next repeated loop, the initial/stored register has the content of the previous loop which is the index value and the value of the first source register); for each of the plurality of source registers (e.g. registers in memory 1, register 5, and specific registers 11x in Figure 4), comparing a value stored in the source register with a value stored in a destination register (e.g. col. 6 lines 1-20); concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the

source register is less than the value stored in the destination register (e.g. step S9 in Figure 3); and wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers; and wherein comparing, concatenating, and storing are implemented by a single processor instruction (e.g. col. 4 lines 45-50 and col. 5 lines 65-68) and performed within a single processor cycle by the network processor (e.g. col. 4 lines 45-50 and col. 5 lines 65-68).

Okumura et al. fail to disclose in Figures 1-9 the step of setting active status bits in the source register and in the destination register such that a value of a register having an active status is less than a value of a register having an inactive status; and wherein each of the plurality of values represents a due timestamp of a corresponding input queue. However, MacInnis et al. disclose in the Figures setting active status bits in the source register and in the destination register (e.g. paragraphs [0038 and 0042] as wherein the register has the status bit built-in) such that a value of a register having an active status is less than a value of a register having an inactive status (e.g. 0/1 as status bit whereas zero is less than one); and wherein each of the plurality of values represents a due timestamp of a corresponding input queue (e.g. paragraph [0035]).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the steps of setting active status bits in the source register and in the destination register such that a value of a register having an active status is less than a value of a register having an inactive status; and wherein each of the plurality of values represents a due timestamp of a corresponding input queue as seen in MacInnnis et al.'s invention into Okumura et al.'s invention because it would enable to

efficiently check the status and prevent unconditional event (e.g. equal result of comparison).

Re claim 20, it is a processor claim having similar limitations as cited in claim 1, except the finding the maximum value (e.g. abstract in Okumura et al.) and the active status is greater than a value of a register having an inactive status (e.g. 1/0 as status bit whereas one is greater than zero). Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 21, it is a processor claim having similar limitations as cited in claim 2, except the finding the maximum value (e.g. abstract in Okumura et al.) and the active status is greater than a value of a register having an inactive status (e.g. 1/0 as status bit whereas one is greater than zero). Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 22, it is a processor claim having similar limitations as cited in claim 3, except the finding the maximum value (e.g. abstract in Okumura et al.) and the active status is greater than a value of a register having an inactive status (e.g. 1/0 as status bit whereas one is greater than zero). Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 23, it is a processor claim having similar limitations as cited in claim 4, except the finding the maximum value (e.g. abstract in Okumura et al.) and the active status is greater than a value of a register having an inactive status (e.g. 1/0 as status bit whereas one is greater than zero). Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 24, it is a processor claim having similar limitations as cited in claim 5, except the finding the maximum value (e.g. abstract in Okumura et al.) and the active status is greater than a value of a register having an inactive status (e.g. 1/0 as status bit whereas one is greater than zero). Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 32, it has similar limitations cited in claim 13 and further Okumura et al. disclose in Figures 1-9 the same architecture can be used/implemented to perform maximum detection in same manner as minimum detection (e.g. col. 5 lines 38-51). Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 33, it has similar limitations cited in claim 13. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

5. Claims 16-19 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (U.S. 5,726,923) in view of MacInnis et al. (U.S. 2003/0185305 A1) and further in view of the admitted prior art.

Re claim 16, Okumura et al. fail to disclose in Figures 1-9 the plurality of values representing a due timestamp of a corresponding input queue is used for implementing Weighted Fair Queuing. However, the admitted prior art discloses the plurality of values representing a due timestamp of a corresponding input queue is used for implementing Weighted Fair Queuing (e.g. page 2 lines 1-26).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the plurality of values representing a due timestamp of a corresponding input queue is used for implementing Weighted Fair Queuing as seen in the admitted prior art into the Okumura et al.'s invention because it would enable to process the data in prioritization for used in network processor (e.g. page 2 lines 1-5 and lines 14-18).

Re claim 17, Okumura et al. disclose in Figures 1-9 a customer premise equipment (e.g. Figure 1 as general architecture) comprising: and a processor operably connected to the interfaces and being adapted to (e.g. for getting data into memory 1 in Figure 1): compare (e.g. by arithmetic logic unit 4 in Figure 1) a first value stored in a first source register of the processor (e.g. specific register 11 in Figure 1) with a second value stored in a second source register of the processor (e.g. registers 5-6 in Figure 1); store the first value in a first destination register of the processor when the first value is less than or equal to the second value (e.g. path when the specific register 11 is less than register 5 in Figure 3); and store the second value in the first destination register of the processor (e.g. value in register 6 in Figure 1) and an index value in a second destination register of the processor (e.g. corresponding index value of register 6 in Figure 1) when the second value is less than the first value (e.g. step S9 in Figure 3), the index value representing the second source register (e.g. Figure 2).

Okumura et al. fail to disclose (1) a network interface operably connected to a first network segment and a network interface operably connected to a second network segment and the condition of equal to for the first test in combine with less than to form

less than or equal to; (2) wherein the first source register and the second source register both include a status identifier for indicating whether the respective register is active or inactive, wherein the status identifier comprises the least significant bit of the value in each respective register. However, the admitted prior art disclose the general architecture of processor operation in network (e.g. pages 1-2) in which a network interface operably connected to a first network segment a network interface operably connected to a second network segment are standard and well-known and the condition less than or equal is very well-known in the art and widely used in many practical applications. Further, MacInnis et al. disclose (2) wherein the first source register and the second source register both include a status identifier for indicating whether the respective register is active or inactive (e.g. paragraphs [0038 and 0042] as wherein the register has the status bit built-in), wherein the status identifier comprises the least significant bit of the value in each respective register (e.g. 0/1 as status bit whereas zero is less than one).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add (1) a network interface operably connected to a first network segment and a network interface operably connected to a second network segment and the condition of equal to for the first test in combine with less than to form less than or equal to; (2) wherein the first source register and the second source register both include a status identifier for indicating whether the respective register is active or inactive, wherein the status identifier comprises the least significant bit of the value in each respective register as seen logically in the admitted prior art and MacInnis et al.'s

invention into Okumura et al.'s invention because it would enable to efficiently check the status and prevent unconditional event with all conditional events (e.g. page 2 lines 1-26).

Re claim 18, it has similar limitations cited in claim 2. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 19, it has similar limitations cited in claim 16. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 35, it has similar limitations cited in claim 16. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 36, it has similar limitations cited in claim 17 and further Okumura et al. disclose in Figures 1-9 the same architecture can be used/implemented to perform maximum detection in same manner as minimum detection (e.g. col. 5 lines 38-51). Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 17.

Re claim 37, it has similar limitations cited in claim 18. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 18.

Re claim 38, it has similar limitations cited in claim 19. Thus, claim 38 is also rejected under the same rationale as cited in the rejection of rejected claim 19.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5, 13, 16-24, 32-33 and 35-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

July 28, 2009